

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1-6. (*Cancelled*).

7. (*Currently Amended*) A clock control circuit comprising:

[[a)] a stage to which a plurality of clocks of mutually different phases are input, this stage generating a plurality of control signals corresponding to transition timing of one clock of the plurality of clocks and to phase differences between the clocks;

[[b)] a switch group, whose switching is controlled by the control signals, for ~~of~~ controlling charging and discharging of a capacitor;

[[c)] a stage of converting terminal voltage of the capacitor to a logic signal and outputting the logic signal; and

[[d)] a stage of varying charging or ~~and~~ discharging speed of the capacitor by shifting switching control timings of switches in said switch group; and

~~(e) a timing dividing circuit that outputs a clock signal having a phase difference obtained by internally dividing the phase difference between the clocks.~~

8-59. (*Cancelled*).